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| Tool Version : Vivado v.2017.4 (lin64) Build 2086221 Fri Dec 15 20:54:30 MST 2017
| Date         : Tue Aug 21 21:56:16 2018
| Host         : tulipp-VirtualBox running 64-bit unknown
| Command      : report_timing_summary -slack_lesser_than 0 -file dr_timing_summary.rpt
| Design       : design_1_wrapper
| Device       : 7z030-sbg485
| Speed File   : -1  PRODUCTION 1.11 2014-09-11
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Timing Summary Report

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| Timer Settings
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  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No
  Ignore I/O Paths                           :  No
  Timing Early Launch at Borrowing Latches   :  false

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes
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check_timing report

Table of Contents

1. checking no_clock

There are 0 register/latch pins with no clock.

2. checking constant_clock

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock

There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints

There are 0 pins that are not constrained for maximum delay.

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay

There are 0 input ports with no input delay specified.

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay

There are 16 ports with no output delay specified. (HIGH)

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock

There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks

There are 0 generated clocks that are not connected to a clock source.

9. checking loops

There are 0 combinational loops in the design.

10. checking partial_input_delay

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay

There are 0 ports with partial output delay specified.

12. checking latch_loops

There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary
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WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
-3.650	-14.254	5	15890	0.015	0.000	0	15744	4.090	0.000	0	7460

Timing constraints are not met.

| Clock Summary
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Clock	Waveform(ns)	Period(ns)	Frequency(MHz)
clk_fpga_0	{0.000 5.000}	10.000	100.000
clk_fpga_1	{0.000 6.749}	13.499	74.080

| Intra Clock Table
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Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
clk_fpga_0	4.485	0.000	0	5532	0.060	0.000	0	5532	4.090	0.000	0	2565
clk_fpga_1	4.980	0.000	0	10174	0.015	0.000	0	10174	5.969	0.000	0	4895

| Inter Clock Table

From Clock	To Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints
clk_fpga_1	clk_fpga_0	12.538	0.000	0	70				
clk_fpga_0	clk_fpga_1	9.092	0.000	0	76				

| Other Path Groups Table

Path Group	From Clock	To Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints
async_default	clk_fpga_0	clk_fpga_0	8.086	0.000	0	32	0.470	0.000	0	32
async_default	clk_fpga_1	clk_fpga_0	-3.650	-10.770	3	3	0.576	0.000	0	3
async_default	clk_fpga_0	clk_fpga_1	-1.742	-3.484	2	2	0.088	0.000	0	2
async_default	clk_fpga_1	clk_fpga_1	10.011	0.000	0	4	0.368	0.000	0	4

| Timing Details

From Clock: clk_fpga_0
To Clock: clk_fpga_0

Setup : 0 Failing Endpoints, Worst Slack 4.485ns, Total Violation 0.000ns
Hold : 0 Failing Endpoints, Worst Slack 0.060ns, Total Violation 0.000ns
PW : 0 Failing Endpoints, Worst Slack 4.090ns, Total Violation 0.000ns
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Pulse Width Checks

Clock Name: clk_fpga_0
Waveform(ns): { 0.000 5.000 }
Period(ns): 10.000
Sources: { design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0] }

Check Type Corner Lib Pin Reference Pin Required(ns) Actual(ns) Slack(ns) Location Pin

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From Clock: clk_fpga_1
To Clock: clk_fpga_1

Setup : 0 Failing Endpoints, Worst Slack 4.980ns, Total Violation 0.000ns
Hold : 0 Failing Endpoints, Worst Slack 0.015ns, Total Violation 0.000ns
PW : 0 Failing Endpoints, Worst Slack 5.969ns, Total Violation 0.000ns
---

Pulse Width Checks

Clock Name: clk_fpga_1
Waveform(ns): { 0.000 6.749 }
Period(ns): 13.499
Sources: { design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[1] }

Check Type Corner Lib Pin Reference Pin Required(ns) Actual(ns) Slack(ns) Location Pin

---
From Clock: clk_fpga_1
To Clock: clk_fpga_0

Setup : 0 Failing Endpoints, Worst Slack 12.538ns, Total Violation 0.000ns
Hold : NA Failing Endpoints, Worst Slack NA , Total Violation NA

From Clock: clk_fpga_0
To Clock: clk_fpga_1

Setup : 0 Failing Endpoints, Worst Slack 9.092ns, Total Violation 0.000ns
Hold : NA Failing Endpoints, Worst Slack NA , Total Violation NA

Path Group: **async_default**
From Clock: clk_fpga_0
 To Clock: clk_fpga_0

Setup : 0 Failing Endpoints, Worst Slack 8.086ns, Total Violation 0.000ns
Hold : 0 Failing Endpoints, Worst Slack 0.470ns, Total Violation 0.000ns
---

Path Group: **async_default**
From Clock: clk_fpga_1
 To Clock: clk_fpga_0

Setup : 3 Failing Endpoints, Worst Slack -3.650ns, Total Violation -10.770ns
Hold : 0 Failing Endpoints, Worst Slack 0.576ns, Total Violation 0.000ns
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Max Delay Paths

Slack (VIOLATED) : -3.650ns (required time - arrival time)
 Source:
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.power_on_rd_rst_reg[0]/C
  (rising edge-triggered cell FDRE clocked by clk_fpga_1 {rise@0.000ns fall@6.749ns period=13.499ns})
 Destination:
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/gf36e1_inst.sngfifo36e1/RST
  (recovery check against rising-edge clock clk_fpga_0 {rise@0.000ns fall@5.000ns period=10.000ns})
 Path Group: **async_default**
 Path Type: Recovery (Max at Slow Process Corner)
 Requirement: 0.004ns (clk_fpga_0 rise@6790.000ns - clk_fpga_1 rise@6789.997ns)
 Data Path Delay: 1.217ns (logic 0.361ns (29.670%) route 0.856ns (70.330%))
 Logic Levels: 1 (LUT2=1)
 Clock Path Skew: -0.176ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 2.335ns = (6792.334 - 6790.000)
  Source Clock Delay (SCD): 2.511ns = (6792.508 - 6789.997)
  Clock Pessimism Removal (CPR): 0.000ns
 Clock Uncertainty: 0.254ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.504ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Clock Domain Crossing: Inter clock paths are considered valid unless explicitly excluded by timing constraints such as set_clock_groups or set_false_path.

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clk_fpga_1 rise edge)		6789.997	6789.997 r
PS7_X0Y0	PS7		0.000	6789.997 r design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[1]
	net (fo=1, routed)	0.936	6790.933	design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[1]
BUFGCTRL_X0Y16	BUFG (Prop_bufg_I_O)	0.120	6791.053 r	design_1_i/processing_system7_0/inst/buffer_fclk_clk_1.FCLK_CLK_1_BUFG/O
	net (fo=4898, routed)	1.455	6792.508	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/m_axis_mm2s_aclk
SLICE_X26Y90	FDRE			r design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.power_on_rd_rst_reg[0]/C
SLICE_X26Y90	FDRE (Prop_fdre_C_Q)	0.308	6792.816 f	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.power_on_rd_rst_reg[0]/Q
	net (fo=1, routed)	0.299	6793.115	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/power_on_rd_rst[0]
SLICE_X27Y91	LUT2 (Prop_lut2_I1_O)	0.053	6793.168 f	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/gf36e1_inst.sngfifo36e1_i_2/O
	net (fo=3, routed)	0.557	6793.725	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/RST
RAMB36_X2Y18	FIFO36E1			f design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/gf36e1_inst.sngfifo36e1/RST

(clock clk_fpga_0 rise edge)
6790.000 6790.000 r
PS7_X0Y0 PS7 0.000 6790.000 r
design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
net (fo=1, routed) 0.903 6790.903
design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
BUFGCTRL_X0Y17 BUFG (Prop_bufg_I_O) 0.113 6791.016 r
design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
net (fo=2566, routed) 1.319 6792.334
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/m_axi_mm2s_aclk
RAMB36_X2Y18 FIFO36E1 r
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/gf36e1_inst.sngfifo36e1/WRCLK
clock pessimism 0.000 6792.334
clock uncertainty -0.254 6792.080
RAMB36_X2Y18 FIFO36E1 (Recov_fifo36e1_WRCLK_RST)
-2.006 6790.074
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/v7_bi_fifo.fblk/gextw[3].gnll_fifo.inst_extd/gonep.inst_prim/gf36e1_inst.sngfifo36e1
---
required time 6790.074
arrival time -6793.724
---
slack -3.650

Path Group: **async_default**
From Clock: clk_fpga_0
To Clock: clk_fpga_1

Setup : 2 Failing Endpoints, Worst Slack -1.742ns, Total Violation -3.484ns
Hold : 0 Failing Endpoints, Worst Slack 0.088ns, Total Violation 0.000ns

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Max Delay Paths

Slack (VIOLATED) : -1.742ns (required time - arrival time)
Source:
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.s_axis_fifo_ainit_nosync_reg_reg/C

(rising edge-triggered cell FDSE clocked by clk_fpga_0 {rise@0.000ns fall@5.000ns period=10.000ns})
Destination: design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.rd_rst_reg1_reg/PRE
(recovery check against rising-edge clock clk_fpga_1 {rise@0.000ns fall@6.749ns period=13.499ns})
Path Group: **async_default**
Path Type: Recovery (Max at Slow Process Corner)
Requirement: 0.016ns (clk_fpga_1 rise@6520.017ns - clk_fpga_0 rise@6520.000ns)
Data Path Delay: 1.135ns (logic 0.269ns (23.706%) route 0.866ns (76.294%))
Logic Levels: 0
Clock Path Skew: -0.152ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.361ns = (6522.377 - 6520.017)
Source Clock Delay (SCD): 2.513ns = (6522.513 - 6520.000)
Clock Pessimism Removal (CPR): 0.000ns
Clock Uncertainty: 0.254ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.504ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns
Clock Domain Crossing: Inter clock paths are considered valid unless explicitly excluded by timing constraints such as set_clock_groups or set_false_path.

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clk_fpga_0 rise edge)		6520.000	6520.000 r
PS7_X0Y0	PS7		0.000	6520.000 r design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
	net (fo=1, routed)	0.936	6520.936	design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
BUFGCTRL_X0Y17	BUFG (Prop_bufg_I_O)	0.120	6521.056 r	design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
	net (fo=2566, routed)	1.457	6522.513	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/m_axi_mm2s_aclk
SLICE_X25Y94	FDSE			r design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.s_axis_fifo_ainit_nosync_reg_reg/C
SLICE_X25Y94	FDSE (Prop_fdse_C_Q)	0.269	6522.782 f	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.s_axis_fifo_ainit_nosync_reg_reg/Q
	net (fo=2, routed)	0.866	6523.648	design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_builtin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/s_axis_fifo_ainit_nosync_reg
SLICE_X27Y94	FDPE			f design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_

NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_b
uiltin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.rd_rst_reg1_reg/PRE
  -- -------------------

                    (clock clk_fpga_1 rise edge)
                                        6520.017 6520.017 r
    PS7_X0Y0   PS7   0.000 6520.017 r
design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[1]
                    net (fo=1, routed)   0.903 6520.919
design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[1]
    BUFGCTRL_X0Y16   BUFG (Prop_bufg_I_O)   0.113 6521.032 r
design_1_i/processing_system7_0/inst/buffer_fclk_clk_1.FCLK_CLK_1_BUFG/O
                    net (fo=4898, routed)   1.345 6522.377
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_
NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_b
uiltin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/m_axis_mm2s_aclk
    SLICE_X27Y94   FDPE   r
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_
NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_b
uiltin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.rd_rst_reg1_reg/C
                    clock pessimism   0.000 6522.377
                    clock uncertainty   -0.254 6522.123
    SLICE_X27Y94   FDPE (Recov_fdpe_C_PRE)   -0.217 6521.906
design_1_i/axi_vdma_0/U0/GEN_SPRT_FOR_MM2S.MM2S_LINEBUFFER_I/GEN_LINEBUF_
NO_SOF.GEN_LINEBUFFER.GEN_ASYNC_FIFO.LB_BUILT_IN.I_LINEBUFFER_FIFO/fg_b
uiltin_fifo_inst/inst_fifo_gen/gconvfifo.rf/gbi.bi/g7ser_birst.rstbt/rsync.ric.rd_rst_reg1_reg
  ----
                    required time   6521.906
                    arrival time   -6523.647
  ----
                    slack   -1.742

Path Group: **async_default**
From Clock: clk_fpga_1
  To Clock: clk_fpga_1

Setup :   0 Failing Endpoints, Worst Slack   10.011ns, Total Violation   0.000ns
Hold :   0 Failing Endpoints, Worst Slack   0.368ns, Total Violation   0.000ns

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